10/20/03
image

AF/2823

Express Mail Label No. EL995580585US

PATENT APPLICATION
Docket No. 11675.106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:		
	John H. Givens	
Serial No.:	08/801,812	
Filed:	February 14, 1997	Art Unit 2823
For:	UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE	
Confirmation No.:	6774	
Examiner:	Julio Maldonado	

CERTIFICATE OF EXPRESS MAIL UNDER 37 C.F.R. § 1.10

I hereby certify that the following documents are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 17th day of October 2003.

- Appeal Brief of Appellant
- Credit Card Payment Form PTO-2038 for $330.00
- Transmittal Letter
- Postcard

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellant
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\106\VFW0000002543V001.doc

Express Mail Label No. EL995580585US

PATENT APPLICATION
Docket No. 11675.106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:		)
	John H. Givens	)
Serial No.:	08/801,812	)
Filed:	February 14, 1997	) Art Unit 2823
For:	UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE	)
Confirmation No.:	6774	)
Examiner:	Julio Maldonado	)

TRANSMITTAL OF APPEAL BRIEF UNDER 37 C.F.R. § 1.192

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith in triplicate is a Brief of Appellant for entry in the above-identified application. Appellant has filed a timely Notice of Appeal from the action of the Examiner dated August 18, 2003. Also enclosed are the following:

x A Certificate of Express Mail Under 37 C.F.R. § 1.10

x Credit Card Payment Form PTO-2038 authorizing payment of $330.00 for the filing fee.

---

x The Commissioner is hereby authorized to charge payment of any patent application processing fees under 37 CFR 1.17 associated with this communication or credit any overpayment to Deposit Account No. 23-3178. Duplicate copies of this sheet are attached.

Dated this 17th day of October 2003.

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellant
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\106\VFW0000002543V001.doc

Express Mail Label No. EL995580585US

PATENT APPLICATION
Docket No. 11675.106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:		)
	John H. Givens	)
Serial No.:	08/801,812	)
Filed:	February 14, 1997	) Art Unit 2823
For:	UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE	)
Confirmation No.:	6774	)
Examiner:	Julio Maldonado	)

BRIEF OF APPELLANT

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant, John H. Givens, has filed a timely Notice of Appeal from the action of the Examiner in finally rejecting all of the claims in this application. This brief is being filed under the provisions of 37 C.F.R. § 1.192. The filing fee of $330.00, as set forth in 37 C.F.R. § 1.17(c) is submitted herewith.

10/22/2003 BABRAHA1 00000104 08801812
01 FC:1402 330.00 OP

REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., by way of assignment from John H. Givens, who is the named inventor and is captioned in the present brief. The assignment documents were recorded at Reel No. 8481, Frame 0357 in the United States Patent and Trademark Office on February 14, 1997.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-28 and 36-63 are pending and appealed in the present application. Claims 29-35 have been cancelled.

STATUS OF AMENDMENTS

All amendments have been previously entered.

SUMMARY OF INVENTION

The present invention is directed to a method for manufacturing an interconnect structure. The method comprises forming a recess 18 within a dielectric material 14 situated on a semiconductor lower substrate 22, with the recess extending below a top surface of the dielectric material, and forming a diffusion barrier layer 24 on the recess within the dielectric material (Spec., page 8, lines 15-25; Figs. 1 and 2). A seed layer 26 is formed on the diffusion barrier layer (Spec., page 9, lines 19-20), and the diffusion barrier layer is composed of a material

having a melting point greater than or equal to that of a material from which the seed layer is composed. An electrically conductive layer 28 is formed on the seed layer including the portion of the seed layer within the recess (Spec., page 10, line 18), with the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, and the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed. An energy absorbing layer 30 is formed on the electrically conductive layer (Spec., page 11, lines 5-6), with the energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer. Energy is applied to the energy absorbing layer to cause the electrically conductive layer to flow within the recess. Portions of the energy absorbing layer and the electrically conductive layer are then removed that are situated above the top surface of the dielectric material.

ISSUES

1. Whether claims 1, 3-5, 7-11, and 36-45 are unobvious over U.S. Patent No. 5,847,461 to Xu et al. (hereafter "*Xu* '461") in view of U.S. Patent No. 6,217,721 B1 to Xu et al. (hereafter "*Xu* '721").

2. Whether claims 2, 6, and 12-15 are unobvious over *Xu* '461 in view of *Xu* '721, and further in view of U.S. Patent No. 5,869,395 to Yim (hereafter "*Yim*").

3. Whether claims 16-28 and 57-63 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

4. Whether claims 46-56 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

GROUPING OF CLAIMS

Claims 1-15 and 36-45 stand or fall together. Claims 16-28 and 57-63 stand or fall together. Claims 46-56 stand or fall together.

ARGUMENT

1. Claims 1, 3-5, 7-11, and 36-45 are Unobvious Over *Xu* '461 in View of *Xu* '721

Claims 1, 3-5, 7-11, and 36-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721. For the reasons that follow, Appellant respectfully submits that claims 1, 3-5, 7-11, and 36-45 are unobvious over *Xu* '461 in view of *Xu* '721.

The law is well settled that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-121, -122, 8th ed. (Aug. 2001).

Xu '461 teaches an integrated circuit structure having an insulating layer 10 formed over integrated circuit structure 2. Openings 14 and 16 are formed in insulating layer 10 and extend downwardly from upper surface 12 of the insulating layer 10 to expose surfaces 4 and 6 of integrated circuit structure 2 at the bottom of the openings 14 and 16. A barrier layer 20 is formed over upper surface 12 and insulating layer 10 as well as over the side walls of openings

14 and 16 and over exposed surfaces 4 and 6 at the respective bottoms of openings 14 and 16 (col. 3, lines 12-22). A metal layer 30 comprising a layer of compressively stressed metal is subsequently extruded down into openings 14 and 16 (col. 4, lines 17-23). A cap layer 40 is formed over metal layer 30. The cap layer 40 comprises a high tensile strength material to restrain the upward movement of metal layer 30 during the subsequent extrusion step (col. 6, lines 26-34).

The Examiner cited *Xu* '721 for teaching the formation of a seed layer 164 on a diffusion barrier layer 162 (Fig. 8). The Examiner asserted that it would have an obvious to one of ordinary skill in the art at the time the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer, and having the thermal properties as taught by *Xu* '721 in the interconnect formation method of *Xu* '461, since heating the barrier layer in the nitrogen environment substantially reduces the electronic barrier at the metal-semiconductor interface and the addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures (Office Action, pp. 3-4).

Appellant submits that *Xu* '461 specifically teaches away from using a seed layer, teaching that:

> [A]s dimensions of lines and contact openings decreased, with ever increasing scale of VLSI structures, problems arose with securing satisfactory filling of the entire contact opening with the aluminum used to form the contact layer over the insulating layer. This, in turn, has given rise to the use of other filler materials such as tungsten to fill the contact opening prior to the formation of the aluminum layer over the insulating layer. After formation of, for example, a barrier layer of TiN, a layer of tungsten is deposited over the barrier layer and insulating layer which also fills the contact opening after which the structure is planarized to remove all of the surface tungsten (leaving only the tungsten in the contact openings). The aluminum layer is then formed over the insulating layer which aluminum layer thereby makes electrical contact with the upper exposed surface of the underlying tungsten in the contact opening.
>
> While this approach has solved the problem of adequate filling of small

> contact openings with conductive material, the use of tungsten as a filler material results in other problems. Filling the openings with tungsten adds further deposition and planarization steps to the process, resulting in more complexity, more cost, and less reliability. In addition, the use of tungsten metal results in higher particle formation possibilities, higher resistivity of the tungsten compared to aluminum, and a metal interface wherein the crystallographic disposition of the tungsten can, in turn, affect the crystallographic form of the aluminum subsequently deposited therein, i.e., by the tungsten surface providing a seed surface for the aluminum deposition, thereby sometimes resulting in the subsequent formation of a less desirable crystallographic form of aluminum. It would, therefore, be highly desirable to be able to fill very small diameter openings in an insulation layer with metal such [as] aluminum initially deposited on the surface of the insulating layer and then later patterned to form a metal interconnect layer, i.e., to use the same metal to both fill the openings in the insulation layer and to form the electrically conductive interconnect or wiring harness on the surface of the insulating layer.

Col. 1, line 56 through col. 2, line 27 (emphasis added). Thus, *Xu* '461 specifically teaches that a seed layer is undesirable when filling small openings and is directed toward other methods of filling the contact openings.

Appellant submits that the combination of *Xu* '461 and *Xu* '721 is improper because *Xu* '461 specifically teaches away from the use of a seed layer when extruding conductive material into very small contact openings. Thus, one of skill in the art would not be motivated to apply a seed layer under the metal layer 30 of *Xu* '461 in view of the fact that a seed layer is specifically taught against.

Accordingly, independent claims 1, 36 and 45, as well as dependent claims 3-5, 7-11, and 37-44 would not have been obvious over the cited references since these claims all recite forming a "seed layer" on the diffusion barrier layer. Appellant therefore respectfully requests that the rejection of claims 1, 3-5, 7-11, and 36-45 under 35 U.S.C. § 103(a) be overturned.

2. Claims 2, 6, and 12-15 are Unobvious Over *Xu* '461 in View of *Xu* '721 and *Yim*

Claims 2, 6, and 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721, and further in view of *Yim*. For the reasons that follow, Appellant respectfully submits that claims 2, 6, and 12-15 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

Claims 2, 6, and 12-15 depend from claim 1 and thus incorporate the limitations thereof. As discussed above, there would have been no motivation to combine the teachings of *Xu* '461 and *Xu* '721, since *Xu* '461 teaches away from the use of a seed layer. In addition, *Yim* does not teach or suggest the use of any seed layer. Thus, the further combination of the teachings of *Yim* would fail to achieve the claimed invention. As such, claims 2, 6, and 12-15 are distinguishable over the cited references for at least the same reasons as discussed above with respect to claim 1.

Accordingly, claims 2, 6, and 12-15 would not have been obvious over the cited references. Appellant therefore respectfully requests that the rejection of claims 2, 6, and 12-15 under 35 U.S.C. § 103(a) be overturned.

3. Claims 16-28 and 57-63 are Unobvious Over *Xu* '461 in View of *Xu* '721 and *Yim*

Claims 16-28 and 57-63 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721 and *Yim*. For the reasons that follow, Appellant respectfully submits that claims 16-28 and 57-63 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

Independent claims 16, 23, 24, 28, 57 and 62 all recite depositing or forming "a seed layer" on the diffusion barrier layer. As discussed previously with respect to claim 1, *Xu* '461 teaches away from the use of a seed layer when filling very small openings in interconnect structures. In addition, *Yim* does not teach or suggest the use of any seed layer. Thus, the

combination of the teachings of *Xu* '461 and *Xu* '721 is improper, and the further combination of the teachings of *Yim* would fail to achieve the claimed invention.

Hence, claims 16, 23, 24, 28, 57 and 62, as well as dependent claims 17-22, 25-27, 58-61, and 63, would not have been obvious over the cited references. Appellant therefore respectfully requests that the rejection of claims 16-28 and 57-63 under 35 U.S.C. § 103(a) be overturned.

4. Claims 46-56 are Unobvious Over *Xu* '461 in View of *Xu* '721 and *Yim*

Claims 46-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721 and *Yim*. For the reasons that follow, Appellant respectfully submits that claims 46-56 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

Independent claims 46 and 54 recite forming a "seed layer" upon the diffusion barrier layer. As discussed previously, *Xu* '461 teaches away from the use of a seed layer as disclosed in *Xu* '721. In addition, *Yim* does not teach or suggest the use of any seed layer. Thus, the combination of the teachings of *Xu* '461 and *Xu* '721 is improper, and the further combination of the teachings of *Yim* would fail to achieve the claimed invention.

In addition, claim 46 recites that a second portion of the recess has a height and a uniform width "that is less than the width of the first portion and that is not greater than 25% of the height". The Examiner admits that none of the cited references teach this limitation, but takes official notice that the claimed range is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species (Office Action, p. 11). Appellant respectfully disagrees. Determining the recited range in claim 46 would not be a matter of routine experimentation, since there are many permutations of the width/height of a multi-portion recess that could be formed. Thus, taking official notice with respect to the recited

range in claim 46 is improper since such a range is not "capable of instant and unquestionable demonstration as being well-known." M.P.E.P. § 2144.03 (A).

Hence, independent claims 46 and 54 as well as dependent claims 47-53 and 55-56 would not have been obvious over the cited references. Appellant therefore respectfully requests that the rejection of claims 46-56 under 35 U.S.C. § 103(a) be overturned.

In view of the foregoing, Appellant respectfully requests the Board to overturn the Examiner's rejections of the appealed claims.

Dated this 17th day of October 2003.

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellant
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\106\VFW0000002542V001.doc

APPENDIX: CLAIMS ON APPEAL

1. A method for manufacturing an interconnect structure comprising:

forming a recess within a dielectric material situated on a semiconductor lower substrate, said recess extending below a top surface of said dielectric material;

forming a diffusion barrier layer on the recess within the dielectric material;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

forming an energy absorbing layer on said electrically conductive layer, said energy absorbing layer having a greater thermal absorption capacity than that of said electrically conductive layer;

applying, omnidirectionally, energy to said energy absorbing layer to cause said electrically conductive layer to flow within said recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. A method for manufacturing an interconnect structure as recited in Claim 1, wherein forming a diffusion barrier layer on the recess within the dielectric material is a CVD deposition step.

3. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of ceramics, metallics, and intermetallics.

4. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

5. A method for manufacturing an interconnect structure as recited in Claim 1, further comprising, prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer in an environment substantially containing a nitrogen gas.

6. A method for manufacturing an interconnect structure as recited in Claim 1, wherein depositing a seed layer on the diffusion barrier layer is a CVD deposition step.

7. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of ceramics, metallics, and intermetallics.

8. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

9. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

10. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the energy absorbing layer is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. A method for manufacturing an interconnect structure as recited in Claim 1, wherein applying energy to said energy absorbing layer utilizes a furnace.

12. A method for manufacturing an interconnect structure as recited in Claim 1, wherein removing portions of the energy absorbing layer and the electrically conductive layer is an abrasive planarization step.

13. A method for manufacturing an interconnect structure as recited in Claim 12, wherein removing portions of the energy absorbing layer and the electrically conductive layer is a chemical mechanical planarizing step.

14. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess has an aspect ratio greater than about four (4) to one (1).

15. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of the lower substrate.

16. A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed;

heating, omnidirectionally, the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

17. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

18. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

19. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

20. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the energy absorbing layer is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

21. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the heating, omnidirectionally, the energy absorbing layer is performed with a furnace.

22. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of the lower substrate.

23. A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed,

being is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating with a furnace the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

24. A method for manufacturing an interconnect structure comprising:

forming a dielectric material on a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

patterning and etching the dielectric material so as to form a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer:

having a greater thermal absorption capacity than that of said layer composed of aluminum; and

being composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the layer composed of aluminum;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the dielectric material.

25. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

26. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

27. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the energy absorbing layer is composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

28. A method for manufacturing an interconnect structure comprising:

forming at least one silicon layer on a monocrystalline silicon layer of a semiconductor substrate assembly, said silicon layer being selected from the group consisting of undoped silicon dioxide, doped silicon dioxide, undoped silicate glass, and doped silicate glass, wherein said monocrystalline silicon layer defines a plane;

patterning and etching the at least one silicon dioxide layer so as to form a recess therein, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the at least one silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said at least one silicon layer, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the at least one silicon layer, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer having a greater thermal absorption capacity than that of said layer composed of aluminum and being composed of a material:

having both a higher thermal insulation capacity and electric insulation capacity than aluminum; and

selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the at least one silicon layer.

36. A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess;

forming upon the electrically conductive layer an energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer;

flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer.

37. The method as defined in Claim 36, wherein the melting point of:

the diffusion barrier layer is not less than that of the seed layer and is greater than that of the electrically conductive layer; and

the seed layer is not less than that of the electrically conductive layer.

38. The method as defined in Claim 36, further comprising:

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

39. The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of aluminum; and

the energy absorbing layer is composed of a material selected from the group consisting of titanium nitride, tungsten, and a dielectric substance.

40. The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten, titanium nitride, tantalum, and carbon.

41. The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium nitride, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

42. The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

43. The method as defined in Claim 36, wherein flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer is performed with a furnace.

44. The method as defined in Claim 36, wherein the seed layer comprises multiple layers, each layer in said multiple layers being composed of a material selected from the group consisting of silicon and titanium nitride.

45. A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming a first layer on the seed layer including the portion of the seed layer within said recess;

forming upon the first layer a second layer that can absorb more heat than the first layer;

heating, omnidirectionally, the first and second layers to flow the first layer within the recess by heat.

46. A method for manufacturing an interconnect structure, the method comprising:

forming a dielectric material over a semiconductor substrate and having a top surface;

forming a recess within the dielectric material extending from the top surface of the dielectric material to the semiconductor substrate;

filling the recess with an electrically conductive material, wherein filling the recess with the electrically conductive material further comprises:

forming a diffusion barrier layer in contact with the semiconductor substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the

diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer including the portion of the seed layer within said recess; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed;

wherein the recess includes:

a first portion having an uniform width and extending within the dielectric material to the top surface of the dielectric material;

a second portion having a height and a uniform width that is less than the width of the first portion and that is not greater than 25% of the height, the second portion extending from the semiconductor substrate to terminate at the first portion; and

wherein the filling the recess is performed by causing the electrically conductive material to flow within the recess by applying omnidirectional heating.

47. The method as defined in Claim 46, wherein the first portion is a trench having a bottom surface that extends longitudinally parallel to the top surface of the dielectric material, and the second portion is a contact plug.

48. The method as defined in Claim 46, wherein filling the recess with the electrically conductive material by applying omnidirectional heating is performed with a furnace.

49. The method as defined in Claim 46, wherein the diffusion barrier layer is upon the top surface of the dielectric material.

50. The method as defined in Claim 46, wherein the diffusion barrier layer is composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

51. The method as defined in Claim 46, wherein the seed layer is composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

52. The method as defined in Claim 46, wherein the conductor layer is composed of a material selected from the group consisting of aluminum and copper.

53. The method as defined in Claim 46, wherein the material from which the energy absorbing layer is composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

54. A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess including a contact hole situated below a trench, said contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of said lower substrate; and

forming an electrically conductive layer situated within and filling both the contact hole and the trench and extending to terminate above the planar top surface of the dielectric material;

wherein the filling both the contact hole and the trench is performed by causing the electrically conductive layer to flow into the contact hole and the trench by applying omnidirectional heating; and

wherein forming the electrically conductive layer comprises:

forming a diffusion barrier layer in contact with the lower substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed.

55. The method as defined in Claim 54, wherein forming an electrically conductive layer by applying omnidirectional heating to cause the electrically conductive layer to flow into the contact hole and the trench is performed with a furnace.

56. The method as defined in Claim 54, wherein the contact hole has a height and a width, and the height is greater than four times the width.

57. A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane said lower substrate;

forming a diffusion barrier layer on the trench and the contact hole;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer within the trench and contact hole and extending to terminate at the planar top surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

58. The method as defined in Claim 57, wherein the material from which the diffusion barrier layer is substantially composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

59. The method as defined in Claim 57, wherein the material from which the seed layer is substantially composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

60. The method as defined in Claim 57, wherein the material from which the electrically conductive layer is substantially composed is selected from the group consisting of aluminum and copper.

61. The method as defined in Claim 57, wherein the applying energy to the electrically conductive layer is performed with a furnace.

62. A method for manufacturing an interconnect structure, the method comprising:

providing a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

forming a dielectric material on the monocrystalline silicon layer;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon

layer and terminating at an opposite end thereof at said trench, said contact hole being oriented perpendicular to the plane of said monocrystalline silicon layer, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of said monocrystalline silicon layer;

forming a diffusion barrier layer on the trench and the contact hole, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

forming a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer within the trench and the contact hole and extending to terminate at the planar surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed being selected from the group consisting of aluminum and copper; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

63. The method as recited in Claim 62, wherein the applying energy to the electrically conductive layer is performed with a furnace.

Express Mail Label No. EL995580585US

PATENT APPLICATION
Docket No. 11675.106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND
INTERFERENCES

In re application of:		)
	John H. Givens	)
Serial No.:	08/801,812	)
Filed:	February 14, 1997	) Art Unit 2823
For:	UTILIZATION OF ENERGY ABSORBING LAYER TO IMPROVE METAL FLOW AND FILL IN A NOVEL INTERCONNECT STRUCTURE	)
Confirmation No.:	6774	)
Examiner:	Julio Maldonado	)

BRIEF OF APPELLANT

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant, John H. Givens, has filed a timely Notice of Appeal from the action of the Examiner in finally rejecting all of the claims in this application. This brief is being filed under the provisions of 37 C.F.R. § 1.192. The filing fee of $330.00, as set forth in 37 C.F.R. § 1.17(c) is submitted herewith.

REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., by way of assignment from John H. Givens, who is the named inventor and is captioned in the present brief. The assignment documents were recorded at Reel No. 8481, Frame 0357 in the United States Patent and Trademark Office on February 14, 1997.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-28 and 36-63 are pending and appealed in the present application. Claims 29-35 have been cancelled.

STATUS OF AMENDMENTS

All amendments have been previously entered.

SUMMARY OF INVENTION

The present invention is directed to a method for manufacturing an interconnect structure. The method comprises forming a recess 18 within a dielectric material 14 situated on a semiconductor lower substrate 22, with the recess extending below a top surface of the dielectric material, and forming a diffusion barrier layer 24 on the recess within the dielectric material (Spec., page 8, lines 15-25; Figs. 1 and 2). A seed layer 26 is formed on the diffusion barrier layer (Spec., page 9, lines 19-20), and the diffusion barrier layer is composed of a material

having a melting point greater than or equal to that of a material from which the seed layer is composed. An electrically conductive layer 28 is formed on the seed layer including the portion of the seed layer within the recess (Spec., page 10, line 18), with the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, and the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed. An energy absorbing layer 30 is formed on the electrically conductive layer (Spec., page 11, lines 5-6), with the energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer. Energy is applied to the energy absorbing layer to cause the electrically conductive layer to flow within the recess. Portions of the energy absorbing layer and the electrically conductive layer are then removed that are situated above the top surface of the dielectric material.

ISSUES

1. Whether claims 1, 3-5, 7-11, and 36-45 are unobvious over U.S. Patent No. 5,847,461 to Xu et al. (hereafter "*Xu* '461") in view of U.S. Patent No. 6,217,721 B1 to Xu et al. (hereafter "*Xu* '721").

2. Whether claims 2, 6, and 12-15 are unobvious over *Xu* '461 in view of *Xu* '721, and further in view of U.S. Patent No. 5,869,395 to Yim (hereafter "*Yim*").

3. Whether claims 16-28 and 57-63 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

4. Whether claims 46-56 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

GROUPING OF CLAIMS

Claims 1-15 and 36-45 stand or fall together. Claims 16-28 and 57-63 stand or fall together. Claims 46-56 stand or fall together.

ARGUMENT

1. Claims 1, 3-5, 7-11, and 36-45 are Unobvious Over *Xu* '461 in View of *Xu* '721

Claims 1, 3-5, 7-11, and 36-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721. For the reasons that follow, Appellant respectfully submits that claims 1, 3-5, 7-11, and 36-45 are unobvious over *Xu* '461 in view of *Xu* '721.

The law is well settled that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation ... to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, the "teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (citations omitted) M.P.E.P. §§ 2142, 2143, p. 2100-121, -122, 8th ed. (Aug. 2001).

Xu '461 teaches an integrated circuit structure having an insulating layer 10 formed over integrated circuit structure 2. Openings 14 and 16 are formed in insulating layer 10 and extend downwardly from upper surface 12 of the insulating layer 10 to expose surfaces 4 and 6 of integrated circuit structure 2 at the bottom of the openings 14 and 16. A barrier layer 20 is formed over upper surface 12 and insulating layer 10 as well as over the side walls of openings

14 and 16 and over exposed surfaces 4 and 6 at the respective bottoms of openings 14 and 16 (col. 3, lines 12-22). A metal layer 30 comprising a layer of compressively stressed metal is subsequently extruded down into openings 14 and 16 (col. 4, lines 17-23). A cap layer 40 is formed over metal layer 30. The cap layer 40 comprises a high tensile strength material to restrain the upward movement of metal layer 30 during the subsequent extrusion step (col. 6, lines 26-34).

The Examiner cited *Xu* '721 for teaching the formation of a seed layer 164 on a diffusion barrier layer 162 (Fig. 8). The Examiner asserted that it would have an obvious to one of ordinary skill in the art at the time the invention was made to form a seed layer after the formation of the barrier layer and prior to the formation of the conductive layer, and having the thermal properties as taught by *Xu* '721 in the interconnect formation method of *Xu* '461, since heating the barrier layer in the nitrogen environment substantially reduces the electronic barrier at the metal-semiconductor interface and the addition of titanium nitride as a seed layer improves the flow of aluminum into an interconnect at moderate temperatures (Office Action, pp. 3-4).

Appellant submits that *Xu* '461 specifically teaches away from using a seed layer, teaching that:

> [A]s dimensions of lines and contact openings decreased, with ever increasing scale of VLSI structures, problems arose with securing satisfactory filling of the entire contact opening with the aluminum used to form the contact layer over the insulating layer. This, in turn, has given rise to the use of other filler materials such as tungsten to fill the contact opening prior to the formation of the aluminum layer over the insulating layer. After formation of, for example, a barrier layer of TiN, a layer of tungsten is deposited over the barrier layer and insulating layer which also fills the contact opening after which the structure is planarized to remove all of the surface tungsten (leaving only the tungsten in the contact openings). The aluminum layer is then formed over the insulating layer which aluminum layer thereby makes electrical contact with the upper exposed surface of the underlying tungsten in the contact opening.

While this approach has solved the problem of adequate filling of small

> contact openings with conductive material, the use of tungsten as a filler material results in other problems. Filling the openings with tungsten adds further deposition and planarization steps to the process, resulting in more complexity, more cost, and less reliability. In addition, the use of tungsten metal results in higher particle formation possibilities, higher resistivity of the tungsten compared to aluminum, and a metal interface wherein the crystallographic disposition of the tungsten can, in turn, affect the crystallographic form of the aluminum subsequently deposited therein, i.e., by the tungsten surface providing a seed surface for the aluminum deposition, thereby sometimes resulting in the subsequent formation of a less desirable crystallographic form of aluminum. It would, therefore, be highly desirable to be able to fill very small diameter openings in an insulation layer with metal such [as] aluminum initially deposited on the surface of the insulating layer and then later patterned to form a metal interconnect layer, i.e., to use the same metal to both fill the openings in the insulation layer and to form the electrically conductive interconnect or wiring harness on the surface of the insulating layer.

Col. 1, line 56 through col. 2, line 27 (emphasis added). Thus, *Xu* '461 specifically teaches that a seed layer is undesirable when filling small openings and is directed toward other methods of filling the contact openings.

Appellant submits that the combination of *Xu* '461 and *Xu* '721 is improper because *Xu* '461 specifically teaches away from the use of a seed layer when extruding conductive material into very small contact openings. Thus, one of skill in the art would not be motivated to apply a seed layer under the metal layer 30 of *Xu* '461 in view of the fact that a seed layer is specifically taught against.

Accordingly, independent claims 1, 36 and 45, as well as dependent claims 3-5, 7-11, and 37-44 would not have been obvious over the cited references since these claims all recite forming a "seed layer" on the diffusion barrier layer. Appellant therefore respectfully requests that the rejection of claims 1, 3-5, 7-11, and 36-45 under 35 U.S.C. § 103(a) be overturned.

2. Claims 2, 6, and 12-15 are Unobvious Over *Xu* '461 in View of *Xu* '721 and *Yim*

Claims 2, 6, and 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721, and further in view of *Yim*. For the reasons that follow, Appellant respectfully submits that claims 2, 6, and 12-15 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

Claims 2, 6, and 12-15 depend from claim 1 and thus incorporate the limitations thereof. As discussed above, there would have been no motivation to combine the teachings of *Xu* '461 and *Xu* '721, since *Xu* '461 teaches away from the use of a seed layer. In addition, *Yim* does not teach or suggest the use of any seed layer. Thus, the further combination of the teachings of *Yim* would fail to achieve the claimed invention. As such, claims 2, 6, and 12-15 are distinguishable over the cited references for at least the same reasons as discussed above with respect to claim 1.

Accordingly, claims 2, 6, and 12-15 would not have been obvious over the cited references. Appellant therefore respectfully requests that the rejection of claims 2, 6, and 12-15 under 35 U.S.C. § 103(a) be overturned.

3. Claims 16-28 and 57-63 are Unobvious Over *Xu* '461 in View of *Xu* '721 and *Yim*

Claims 16-28 and 57-63 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721 and *Yim*. For the reasons that follow, Appellant respectfully submits that claims 16-28 and 57-63 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

Independent claims 16, 23, 24, 28, 57 and 62 all recite depositing or forming "a seed layer" on the diffusion barrier layer. As discussed previously with respect to claim 1, *Xu* '461 teaches away from the use of a seed layer when filling very small openings in interconnect structures. In addition, *Yim* does not teach or suggest the use of any seed layer. Thus, the

combination of the teachings of *Xu* '461 and *Xu* '721 is improper, and the further combination of the teachings of *Yim* would fail to achieve the claimed invention.

Hence, claims 16, 23, 24, 28, 57 and 62, as well as dependent claims 17-22, 25-27, 58-61, and 63, would not have been obvious over the cited references. Appellant therefore respectfully requests that the rejection of claims 16-28 and 57-63 under 35 U.S.C. § 103(a) be overturned.

4. Claims 46-56 are Unobvious Over *Xu* '461 in View of *Xu* '721 and *Yim*

Claims 46-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Xu* '461 in view of *Xu* '721 and *Yim*. For the reasons that follow, Appellant respectfully submits that claims 46-56 are unobvious over *Xu* '461 in view of *Xu* '721 and *Yim*.

Independent claims 46 and 54 recite forming a "seed layer" upon the diffusion barrier layer. As discussed previously, *Xu* '461 teaches away from the use of a seed layer as disclosed in *Xu* '721. In addition, *Yim* does not teach or suggest the use of any seed layer. Thus, the combination of the teachings of *Xu* '461 and *Xu* '721 is improper, and the further combination of the teachings of *Yim* would fail to achieve the claimed invention.

In addition, claim 46 recites that a second portion of the recess has a height and a uniform width "that is less than the width of the first portion and that is not greater than 25% of the height". The Examiner admits that none of the cited references teach this limitation, but takes official notice that the claimed range is obvious because it is a matter of determining optimum process conditions by routine experimentation with a limited number of species (Office Action, p. 11). Appellant respectfully disagrees. Determining the recited range in claim 46 would not be a matter of routine experimentation, since there are many permutations of the width/height of a multi-portion recess that could be formed. Thus, taking official notice with respect to the recited

range in claim 46 is improper since such a range is not "capable of instant and unquestionable demonstration as being well-known." M.P.E.P. § 2144.03 (A).

Hence, independent claims 46 and 54 as well as dependent claims 47-53 and 55-56 would not have been obvious over the cited references. Appellant therefore respectfully requests that the rejection of claims 46-56 under 35 U.S.C. § 103(a) be overturned.

In view of the foregoing, Appellant respectfully requests the Board to overturn the Examiner's rejections of the appealed claims.

Dated this 17th day of October 2003.

Respectfully submitted,

Gregory M. Taylor
Attorney for Appellant
Registration No. 34,263
Customer No. 022901

GMT:vfw
W:\11675\106\VFW0000002542V001.doc

APPENDIX: CLAIMS ON APPEAL

1. A method for manufacturing an interconnect structure comprising:

forming a recess within a dielectric material situated on a semiconductor lower substrate, said recess extending below a top surface of said dielectric material;

forming a diffusion barrier layer on the recess within the dielectric material;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

forming an energy absorbing layer on said electrically conductive layer, said energy absorbing layer having a greater thermal absorption capacity than that of said electrically conductive layer;

applying, omnidirectionally, energy to said energy absorbing layer to cause said electrically conductive layer to flow within said recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. A method for manufacturing an interconnect structure as recited in Claim 1, wherein forming a diffusion barrier layer on the recess within the dielectric material is a CVD deposition step.

3. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of ceramics, metallics, and intermetallics.

4. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

5. A method for manufacturing an interconnect structure as recited in Claim 1, further comprising, prior to forming a seed layer on the diffusion barrier layer, heating the diffusion barrier layer in an environment substantially containing a nitrogen gas.

6. A method for manufacturing an interconnect structure as recited in Claim 1, wherein depositing a seed layer on the diffusion barrier layer is a CVD deposition step.

7. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of ceramics, metallics, and intermetallics.

8. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

9. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

10. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the energy absorbing layer is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. A method for manufacturing an interconnect structure as recited in Claim 1, wherein applying energy to said energy absorbing layer utilizes a furnace.

12. A method for manufacturing an interconnect structure as recited in Claim 1, wherein removing portions of the energy absorbing layer and the electrically conductive layer is an abrasive planarization step.

13. A method for manufacturing an interconnect structure as recited in Claim 12, wherein removing portions of the energy absorbing layer and the electrically conductive layer is a chemical mechanical planarizing step.

14. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess has an aspect ratio greater than about four (4) to one (1).

15. A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of the lower substrate.

16. A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed;

heating, omnidirectionally, the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

17. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

18. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

19. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper.

20. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the energy absorbing layer is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

21. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the heating, omnidirectionally, the energy absorbing layer is performed with a furnace.

22. A method for manufacturing an interconnect structure as recited in Claim 16, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of the lower substrate.

23. A method for manufacturing an interconnect structure comprising:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed,

being is composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating with a furnace the energy absorbing layer to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

24. A method for manufacturing an interconnect structure comprising:

forming a dielectric material on a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

patterning and etching the dielectric material so as to form a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer:

having a greater thermal absorption capacity than that of said layer composed of aluminum; and

being composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the layer composed of aluminum;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the dielectric material.

25. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the diffusion barrier layer is composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

26. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the seed layer is composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

27. A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the energy absorbing layer is composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

28. A method for manufacturing an interconnect structure comprising:

forming at least one silicon layer on a monocrystalline silicon layer of a semiconductor substrate assembly, said silicon layer being selected from the group consisting of undoped silicon dioxide, doped silicon dioxide, undoped silicate glass, and doped silicate glass, wherein said monocrystalline silicon layer defines a plane;

patterning and etching the at least one silicon dioxide layer so as to form a recess therein, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the at least one silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said at least one silicon layer, the trench being parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the at least one silicon layer, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer composed of aluminum on the seed layer including the portion of the seed layer within said recess, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum, said energy absorbing layer having a greater thermal absorption capacity than that of said layer composed of aluminum and being composed of a material:

having both a higher thermal insulation capacity and electric insulation capacity than aluminum; and

selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating omnidirectionally with a furnace the energy absorbing layer to cause said layer composed of aluminum to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum that are situated above the top surface of the at least one silicon layer.

36. A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming an electrically conductive layer on the seed layer including the portion of the seed layer within said recess;

forming upon the electrically conductive layer an energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer;

flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer.

37. The method as defined in Claim 36, wherein the melting point of:

the diffusion barrier layer is not less than that of the seed layer and is greater than that of the electrically conductive layer; and

the seed layer is not less than that of the electrically conductive layer.

38. The method as defined in Claim 36, further comprising:

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

39. The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of aluminum; and

the energy absorbing layer is composed of a material selected from the group consisting of titanium nitride, tungsten, and a dielectric substance.

40. The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten, titanium nitride, tantalum, and carbon.

41. The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium nitride, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

42. The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

43. The method as defined in Claim 36, wherein flowing the electrically conductive layer within the recess by omnidirectionally heating the energy absorbing layer is performed with a furnace.

44. The method as defined in Claim 36, wherein the seed layer comprises multiple layers, each layer in said multiple layers being composed of a material selected from the group consisting of silicon and titanium nitride.

45. A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming a first layer on the seed layer including the portion of the seed layer within said recess;

forming upon the first layer a second layer that can absorb more heat than the first layer;

heating, omnidirectionally, the first and second layers to flow the first layer within the recess by heat.

46. A method for manufacturing an interconnect structure, the method comprising:

forming a dielectric material over a semiconductor substrate and having a top surface;

forming a recess within the dielectric material extending from the top surface of the dielectric material to the semiconductor substrate;

filling the recess with an electrically conductive material, wherein filling the recess with the electrically conductive material further comprises:

forming a diffusion barrier layer in contact with the semiconductor substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the

diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer including the portion of the seed layer within said recess; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed;

wherein the recess includes:

a first portion having an uniform width and extending within the dielectric material to the top surface of the dielectric material;

a second portion having a height and a uniform width that is less than the width of the first portion and that is not greater than 25% of the height, the second portion extending from the semiconductor substrate to terminate at the first portion; and

wherein the filling the recess is performed by causing the electrically conductive material to flow within the recess by applying omnidirectional heating.

47. The method as defined in Claim 46, wherein the first portion is a trench having a bottom surface that extends longitudinally parallel to the top surface of the dielectric material, and the second portion is a contact plug.

48. The method as defined in Claim 46, wherein filling the recess with the electrically conductive material by applying omnidirectional heating is performed with a furnace.

49. The method as defined in Claim 46, wherein the diffusion barrier layer is upon the top surface of the dielectric material.

50. The method as defined in Claim 46, wherein the diffusion barrier layer is composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

51. The method as defined in Claim 46, wherein the seed layer is composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

52. The method as defined in Claim 46, wherein the conductor layer is composed of a material selected from the group consisting of aluminum and copper.

53. The method as defined in Claim 46, wherein the material from which the energy absorbing layer is composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

54. A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess including a contact hole situated below a trench, said contact hole terminating at an end thereof at the lower substrate and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane of said lower substrate; and

forming an electrically conductive layer situated within and filling both the contact hole and the trench and extending to terminate above the planar top surface of the dielectric material;

wherein the filling both the contact hole and the trench is performed by causing the electrically conductive layer to flow into the contact hole and the trench by applying omnidirectional heating; and

wherein forming the electrically conductive layer comprises:

forming a diffusion barrier layer in contact with the lower substrate and the dielectric material;

forming a seed layer upon the diffusion barrier layer and composed of a material having a melting point less than that of the material from which the diffusion barrier layer is composed and being selected from a group consisting of ceramics, metallics, and intermetallics;

forming a conductor layer upon the seed layer; and

forming an energy absorbing layer on the conductor layer that is composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the material from which the conductor layer is composed.

55. The method as defined in Claim 54, wherein forming an electrically conductive layer by applying omnidirectional heating to cause the electrically conductive layer to flow into the contact hole and the trench is performed with a furnace.

56. The method as defined in Claim 54, wherein the contact hole has a height and a width, and the height is greater than four times the width.

57. A method for manufacturing an interconnect structure, the method comprising:

forming a lower substrate situated on a semiconductor substrate assembly, said lower substrate defining a plane;

forming a dielectric material on the lower substrate having a planar top surface;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said contact hole being oriented substantially perpendicular to the plane of said lower substrate, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending substantially parallel to the plane said lower substrate;

forming a diffusion barrier layer on the trench and the contact hole;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer within the trench and contact hole and extending to terminate at the planar top surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

58. The method as defined in Claim 57, wherein the material from which the diffusion barrier layer is substantially composed is selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride.

59. The method as defined in Claim 57, wherein the material from which the seed layer is substantially composed is selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide.

60. The method as defined in Claim 57, wherein the material from which the electrically conductive layer is substantially composed is selected from the group consisting of aluminum and copper.

61. The method as defined in Claim 57, wherein the applying energy to the electrically conductive layer is performed with a furnace.

62. A method for manufacturing an interconnect structure, the method comprising:

providing a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

forming a dielectric material on the monocrystalline silicon layer;

forming a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon

layer and terminating at an opposite end thereof at said trench, said contact hole being oriented perpendicular to the plane of said monocrystalline silicon layer, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending parallel to the plane of said monocrystalline silicon layer;

forming a diffusion barrier layer on the trench and the contact hole, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

forming a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer within the trench and the contact hole and extending to terminate at the planar surface of the dielectric material, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed being selected from the group consisting of aluminum and copper; and

applying, omnidirectionally, energy to the electrically conductive layer to cause the electrically conductive layer to flow within the recess.

63. The method as recited in Claim 62, wherein the applying energy to the electrically conductive layer is performed with a furnace.